IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Daniel Yellin et al. Art Unit: 2133
Serial No.: 10/829,075 Examiner: Joseph D. Torres
Filed : April 21, 2004
Assignee : Intel Corporation
Title : LOW COMPLEXITY CHANNEL DECODERS

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made with a Request for Continued Examination (RCE). No fee is required.

Desig. ID "AA" is the publication for a related application, U.S. patent application no. 09/880,707 (hereafter referred to as '707). Desig. IDs "AB-AG" and "AR-AS" were cited by the Examiner in an Office Action mailed on May 20, 2004 in the related application '707. Desig. IDs "AP-AQ" are mentioned in the section of the specification entitled "BACKGROUND", pages 2-3.

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

Please apply any credits or additional charges to deposit account 06-1050.

Respectfully submitted,

/BY
BING AI
REG. NO. 43,312

Date: April 13, 2007

Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
USPTO Customer No. **20985**
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10726758.doc

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-449002	Application No. 10/829,075
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Daniel Yellin et al.	
		Filing Date April 21, 2004	Group Art Unit 2133

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0194567	12/2002	Yellin et al.			
	AB	5,983,384	11/1999	Ross			
	AC	6,253,185	06/2001	Arean et al.			
	AD	6,393,072	05/2002	Ross et al.			
	AE	6,516,437	02/2003	Van Stralen et al.			
	AF	6,516,444	02/2003	Maru			
	AG	6,725,409	04/2004	Wolf			
	AH						
	AI						
	AJ						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AK							
	AL							
	AM							
	AN							
	AO							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AP	Bahl, L.R., et al., "Optimal Decoding of Linear Codes for Minimizing Symbol Error Rate", *IEEE Trans. Inform. Theory*, pp. 248-287, March 1974.
	AQ	Forney, G.D., "The Viterbi Algorithm", *Proc. IEEE*, 61(3):268-278, March 1973.
	AR	Smit, G., et al., "Mapping the SISO module of the Turbo decoder to a FPFA", *Proc. of Second International Symposium on Mobile Multimedia Systems & Applications (MMSA2000)*, pp. 165-172, November 2000.
	AS	Yeo, E., et al., "VLSI Architecture for Iterative Decoders in Magnetic Recording Channels", *IEEE Transactions on Magnetics*, 37(2):748-755, March 2000.
	AT	

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.